04/13/04

PTO/SB/08 (10-92)
Sheet 1 of 1.

| FORM PTO-1449 | Docket Number (Optional) 008226/DSM/BCVD/JW | Application Number 10/824,313 |
|---|---|---|
| INFORMATION DISCLOSURE CITATION | Applicant(s): Zhenjiang Cui, Jun Zhao, Rick J. Roberts, Shulin Wang, Errol A. C. Sanchez, and Aihua Chen | |
| IN AN APPLICATION (Use several sheets if necessary) | Filing Date 04/13/2004 | Group Art Unit 2823 |

**U.S. PATENT DOCUMENTS**

| EXAMINER INITIAL | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE IF APPROPRIATE |
|---|---|---|---|---|---|---|
| K.N. | 5 0 0 3 1 7 8 | 3/26/91 | Livesay | 250 | 492.3 | Nov. 14, 1988 |
| K.N. | 6 4 0 7 3 9 9 | 6/18/02 | Livesay | 250 | 492.3 | Sep. 30, 1999 |

| | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUBCLASS | Translation YES | Translation NO |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | | | | | |

**OTHER DOCUMENTS** (Including Author, Title, Date, Pertinent Pages, Etc.)

| | | |
|---|---|---|
| K.N. | | S. Inaba et al. "Increase of Parasitic Resistance of Shallow p+ Extension with SiN Sidewall Process by Hydrogen Passivation of Boron and Its Improvement by Preamorphization for Sub-0.25 μm pMOSFETs" 1996 Symp. on VLSI Tech. Dig. of Technical Papers, 1996, pp. 168-169 |
| K.N. | | S. Inaba et al. "Increase of Parasitic Resistance in Shallow p+ Extension with SiN Sidewall Process and Its Improvement by Ge Preamorphization for Sub-0.25 μm pMOSFETs" IEEE Trans. Electr. Dev., Vol. 46, No. 6, June 1999, pp. 1218-1224 |
| K.N. | | M. Tanaka et al. "Realization of High Performance Dual Gate DRAMs without Boron Penetration by Application of Tetrachlorosilane Silicon Nitride Films" 2001 Symp. on VLSI Tech. Dig. of Technical Papers, 2001 |

| EXAMINER | DATE CONSIDERED |
|---|---|
| K Thiemmagaren | 11/17/04 |

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.